In The Claims:

Claims 1 through 7. (Cancelled).

8. (Currently Amended) ~~The apparatus of claim 1 wherein~~ An apparatus for implementing a multi-level system model, comprising:

a picokernel configured to schedule and execute one or more selected processes in an electronic device, said one or more selected processes including an isochronous process and a plesiochronous process; and

a processor coupled to said electronic device for controlling said picokernel, said picokernel ~~includes~~ including an isochronous scheduler and a plesiochronous scheduler, said picokernel responsively invoking said isochronous scheduler in response to an isochronous cycle start signal to thereby select, schedule, and execute active isochronous processes on said electronic device, said active isochronous processes selectively generating flags to designate active plesiochronous processes, said plesiochronous scheduler then selecting, scheduling, and executing said active plesiochronous processes when all of said active isochronous processes have been executed.

Claims 9 through 12. (Cancelled).

13. (Currently Amended) ~~The apparatus of claim 9 wherein~~ An apparatus for implementing a multi-level system model, comprising:

a picokernel configured to schedule and execute one or more selected processes in an electronic device, said one or more selected processes including an isochronous process and a plesiochronous process; and

a processor coupled to said electronic device for controlling said picokernel, said picokernel being stored in a memory device that also includes at least one of device software, a cantaloupe manager, one or more cantaloupes, one or more endochronous application program interfaces, one or more isochronous process representations, and one or more plesiochronous process representations, said one or more isochronous process representations and said one or more plesiochronous process representations each ~~includes~~ including one or more data structures that correspond to a respective process that has been instantiated on said electronic device, said data structures including optimized information for deterministically executing said respective process.

Claims 14 through 23. (Cancelled).

24. (Previously Presented) An apparatus for implementing a multi-level system model, comprising:

a picokernel configured to schedule and execute one or more selected processes in an electronic device, said picokernel detecting a cycle start signal from an isochronous clock to signify a start of an isochronous cycle, said picokernel determining whether one or more active isochronous processes are ready to be executed on said electronic device by referencing an isochronous process list, said picokernel invoking an isochronous scheduler when said one or more active isochronous processes are ready to be executed, said picokernel invoking a plesiochronous scheduler when said one or more active isochronous processes are not ready to be executed, said isochronous scheduler performing a selection procedure on said one or more active isochronous processes to produce a selected isochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said isochronous process, said isochronous scheduler scheduling and executing said selected isochronous process on said electronic device, said selected isochronous process setting a plesiochronous flag to thereby designate an active plesiochronous process for scheduling and execution on said electronic device, said active isochronous process notifying said picokernel which responsively adds a corresponding plesiochronous process identifier to a plesiochronous process list; and

a processor coupled to said electronic device for controlling said picokernel.

Claim 25. (Cancelled).

26. (Currently Amended) ~~The apparatus of claim 1 wherein~~ An apparatus for implementing a multi-level system model, comprising:

a picokernel configured to schedule and execute one or more selected processes in an electronic device, said one or more selected processes including an isochronous process and a plesiochronous process; and

a processor coupled to said electronic device for controlling said picokernel, said picokernel ~~waits~~ waiting until all isochronous processes for a current isochronous cycle have been executed, said picokernel then determining whether one or more active flagged plesiochronous processes are ready to be executed on said electronic device by referencing a plesiochronous process list.

27. (Original) The apparatus of claim 26 wherein said picokernel invokes a plesiochronous scheduler when said one or more active flagged plesiochronous processes are ready to be executed, and wherein said picokernel waits for a new cycle start signal when said one or more active flagged plesiochronous processes are not ready to be executed.

28. (Original) The apparatus of claim 27 wherein said plesiochronous scheduler performs a selection procedure on said one or more active flagged plesiochronous processes to produce a selected plesiochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said plesiochronous process, said plesiochronous scheduler then scheduling and executing said selected plesiochronous process on said electronic device.

29. (Previously Presented) An apparatus for implementing a multi-level system model, comprising:

a picokernel configured to schedule and execute one or more selected processes in an electronic device, said picokernel waiting until all isochronous processes for a current isochronous cycle have been executed, said picokernel then determining whether one or more active flagged plesiochronous processes are ready to be executed on said electronic device by referencing a plesiochronous process list, said picokernel invoking a plesiochronous scheduler when said one or more active flagged plesiochronous processes are ready to be executed, said picokernel waiting for a new cycle start signal when said one or more active flagged plesiochronous processes are not ready to be executed, said plesiochronous scheduler performing a selection procedure on said one or more active flagged plesiochronous processes to produce a selected plesiochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said plesiochronous process, said plesiochronous scheduler then scheduling and executing said selected plesiochronous process on said electronic device, said picokernel halting said plesiochronous process and marking said plesiochronous process for a subsequent completion in response to an interrupt event, said interrupt event including one of a cycle start signal and an exochronous interrupt, said picokernel beginning a new isochronous cycle in response to said cycle start signal, said picokernel switching to an exochronous processing for executing required system tasks in response to said exochronous interrupt; and

a processor coupled to said electronic device for controlling said picokernel.

30. (Currently Amended) ~~The apparatus of claim 28 wherein~~ An apparatus for implementing a multi-level system model, comprising:

a picokernel configured to schedule and execute one or more selected processes in an electronic device, said one or more selected processes including an isochronous process and a plesiochronous process; and

a processor coupled to said electronic device for controlling said picokernel, said picokernel waiting until all isochronous processes for a current isochronous cycle have been executed, said picokernel then determining whether one or more active flagged plesiochronous processes are ready to be executed on said electronic device by referencing a plesiochronous process list, said picokernel invoking a plesiochronous scheduler when said one or more active flagged plesiochronous processes are ready to be executed, said picokernel waiting for a new cycle start signal when said one or more active flagged plesiochronous processes are not ready to be executed, said plesiochronous scheduler performing a selection procedure on said one or more active flagged plesiochronous processes to produce a selected plesiochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said plesiochronous process, said plesiochronous scheduler then scheduling and executing said selected plesiochronous process on said electronic device, said picokernel sequentially ~~selects, schedules, and executes~~ selecting, scheduling, and executing a series of plesiochronous processes using said plesiochronous scheduler, said picokernel returning to wait for said new cycle start signal when all of said series of plesiochronous processes have been executed.

Claims 31 through 37. (Cancelled).

38. (Currently Amended) ~~The method of claim 31 wherein~~ A method for implementing a multi-level system model, comprising the steps of:

scheduling one or more selected processes in an electronic device by using a picokernel, said one or more selected processes including an isochronous process and a plesiochronous process;

executing said one or more selected processes by using said picokernel; and

controlling said picokernel by using a processor, said picokernel ~~includes~~ including an isochronous scheduler and a plesiochronous scheduler, said picokernel responsively invoking said isochronous scheduler in response to an isochronous cycle start signal to thereby select, schedule, and execute active isochronous processes on said electronic device, said active isochronous processes selectively generating flags to designate active plesiochronous processes, said plesiochronous scheduler then selecting, scheduling, and executing said active plesiochronous processes when all of said active isochronous processes have been executed.

Claims 39 through 42. (Cancelled).

43. (Currently Amended) ~~The method of claim 39 wherein~~ A method for implementing a multi-level system model, comprising the steps of:

scheduling one or more selected processes in an electronic device by using a picokernel, said one or more selected processes including an isochronous process and a plesiochronous process;

executing said one or more selected processes by using said picokernel; and

controlling said picokernel by using a processor, said picokernel being stored in a memory device that also includes at least one of device software, a cantaloupe manager, one or more cantaloupes, one or more endochronous application program interfaces, one or more isochronous process representations, and one or more plesiochronous process representations, said one or more isochronous process representations and said one or more plesiochronous process representations each ~~includes~~ including one or more data structures that correspond to a respective process that has been instantiated on said electronic device, said data structures including optimized information for deterministically executing said respective process.

Claims 44 through 53. (Cancelled).

54. (Previously Presented) A method for implementing a multi-level system model, comprising the steps of:

scheduling one or more selected processes in an electronic device by using a picokernel, said picokernel detecting a cycle start signal from an isochronous clock to signify a start of an isochronous cycle, said picokernel determining whether one or more active isochronous processes are ready to be executed on said electronic device by referencing an isochronous process list, said picokernel invoking an isochronous scheduler when said one or more active isochronous processes are ready to be executed, said picokernel invoking a plesiochronous scheduler when said one or more active isochronous processes are not ready to be executed, said isochronous scheduler performing a selection procedure on said one or more active isochronous processes to produce a selected isochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said isochronous process, said isochronous scheduler scheduling said selected isochronous process on said electronic device, said selected isochronous process setting a plesiochronous flag to thereby designate an active plesiochronous process for scheduling and execution on said electronic device, said active isochronous process notifying said picokernel which responsively adds a corresponding plesiochronous process identifier to a plesiochronous process list;

executing said one or more selected processes by using said picokernel; and

controlling said picokernel by using a processor.

Claim 55. (Cancelled).

56. (Currently Amended) ~~The method of claim 31 wherein~~ A method for implementing a multi-level system model, comprising the steps of:

scheduling one or more selected processes in an electronic device by using a picokernel, said one or more selected processes including an isochronous process and a plesiochronous process;

executing said one or more selected processes by using said picokernel; and

controlling said picokernel by using a processor, said picokernel ~~waits~~ waiting until all isochronous processes for a current isochronous cycle have been executed, said picokernel then determining whether one or more active flagged plesiochronous processes are ready to be executed on said electronic device by referencing a plesiochronous process list.

57. (Original) The method of claim 56 wherein said picokernel invokes a plesiochronous scheduler when said one or more active flagged plesiochronous processes are ready to be executed, and wherein said picokernel waits for a new cycle start signal when said one or more active flagged plesiochronous processes are not ready to be executed.

58. (Original) The method of claim 57 wherein said plesiochronous scheduler performs a selection procedure on said one or more active flagged plesiochronous processes to produce a selected plesiochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said plesiochronous process, said plesiochronous scheduler then scheduling and executing said selected plesiochronous process on said electronic device.

59. (Previously Presented) A method for implementing a multi-level system model, comprising the steps of:

scheduling one or more selected processes in an electronic device by using a picokernel, said picokernel waiting until all isochronous processes for a current isochronous cycle have been executed, said picokernel then determining whether one or more active flagged plesiochronous processes are ready to be executed on said electronic device by referencing a plesiochronous process list, said picokernel invoking a plesiochronous scheduler when said one or more active flagged plesiochronous processes are ready to be executed, said picokernel waiting for a new cycle start signal when said one or more active flagged plesiochronous processes are not ready to be executed, said plesiochronous scheduler performing a selection procedure on said one or more active flagged plesiochronous processes to produce a selected plesiochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said plesiochronous process, said plesiochronous scheduler then scheduling said selected plesiochronous process on said electronic device;

executing said one or more selected processes by using said picokernel, said picokernel halting said plesiochronous process and marking said plesiochronous process for a subsequent completion in response to an interrupt event, said interrupt event including one of a cycle start signal and an exochronous interrupt, said picokernel beginning a new isochronous cycle in response to said cycle start signal, said picokernel switching to an exochronous processing for executing required system tasks in response to said exochronous interrupt; and

controlling said picokernel by using a processor.

60. (Currently Amended) ~~The method of claim 58 wherein~~ A method for implementing a multi-level system model, comprising the steps of:

scheduling one or more selected processes in an electronic device by using a picokernel, said one or more selected processes including an isochronous process and a plesiochronous process;

executing said one or more selected processes by using said picokernel; and

controlling said picokernel by using a processor, said picokernel waiting until all isochronous processes for a current isochronous cycle have been executed, said picokernel then determining whether one or more active flagged plesiochronous processes are ready to be executed on said electronic device by referencing a plesiochronous process list, said picokernel invoking a plesiochronous scheduler when said one or more active flagged plesiochronous processes are ready to be executed, said picokernel waiting for a new cycle start signal when said one or more active flagged plesiochronous processes are not ready to be executed, said plesiochronous scheduler performing a selection procedure on said one or more active flagged plesiochronous processes to produce a selected plesiochronous process based upon selection factors that include one of a relative process importance, a process length, a process function, and a process time-sensitivity of said plesiochronous process, said plesiochronous scheduler then scheduling and executing said selected plesiochronous process on said electronic device, said picokernel sequentially ~~selects, schedules, and executes~~ selecting, scheduling, and executing a series of plesiochronous processes using said plesiochronous scheduler, said picokernel returning to wait for said new cycle start signal when all of said series of plesiochronous processes have been executed.

Claims 61 and 62. (Cancelled).